EE 330 Laboratory 6
Resistors, Bonding Pads, and Pad Frames
Spring 2022

Contents

Objective

The objective of this experiment is to investigate the design and layout of resistors, the basic bonding pads that comprise a pad frame, and diodes. Then these will be combined into a basic pad protection circuit.

Checkpoints

The checkpoints for this lab are as follows:

1. Extracted $5k\Omega$ Resistor
2. Diode Layout
3. Bonding Pad (w/ Measurements)
4. LVS Match for ESD Circuit
5. Transient Analysis Proving ESD Class

As with all future labs, these checkpoints must be shown to a lab TA before the end of your next lab section. You should include these checkpoints in your lab report.

Part 1: Layout of a resistor

A resistor can be created using almost any layer available in the process. For example, in the ON 0.5µm process, a rectangular poly resistor can be created by drawing a rectangular poly region with terminals at its ends as shown in Figure 1. The value of this resistor will be the product of the sheet resistance times the number of squares (Note: A corner counts as 0.55 squares). The resistor is often shaped to reduce the overall area, often making a U shape or serpentine for larger resistances.

Since a layout pattern with contacts on two ends can be used for either an interconnect or for a resistor, and since the same physical devices are used for both, the CAD tools have no way of determining strictly from the layout of the resistor what is intended to be a resistor that appears in a circuit schematic and what is intended to be an interconnect which shows no resistance in a schematic. To allow the CAD tools to correctly recognize the regions that correspond to resistors in a circuit schematic, an identification cover called *res_id* is added at layout that covers all regions that are to correspond to resistors in the circuit schematic. A *res_id* cover is shown in Figure 1. The *res_id* cover is an identification layer, not an additional physical layer. The *res_id* cover does not alter the fabrication process.

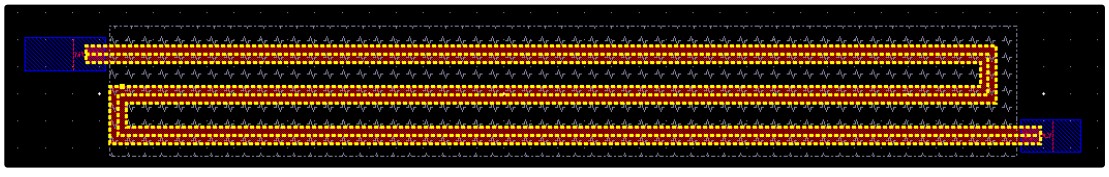


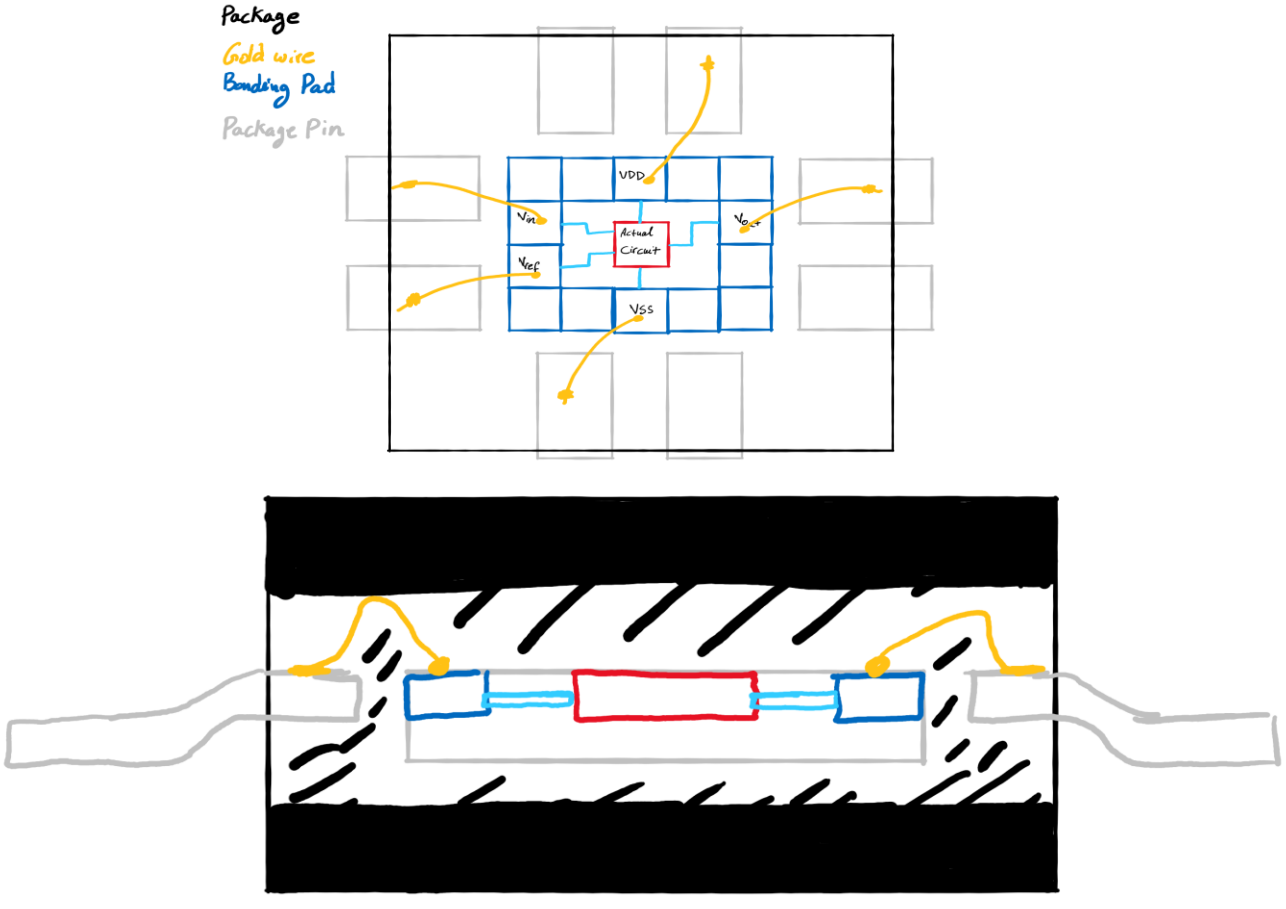
Figure 1: Resistor layout utilizing serpentine poly, metal interconnects, and res_id.

Part 1.1 Create a resistor layout

Create a resistor of 5 kΩ (+/- 1%) inside a rectangular boundary using any layer. Make sure that the diagonal of a bounding rectangle is reasonably small. Use the parameters included in Appendix 1 for this design. Extract the resistor to compare the extracted value with the design value (the extracted view should have a box that says “Res”, when you press Shift+F this will show the resistance value).

Part 2: Introduction to bonding pads

A bonding pad is used as part of the connection of the circuit on a die to a pin on a package. One side of a wire (often gold) connects to the bonding pad while the other side connects to the corresponding pin on a package. This interconnecting wire is called a "bonding wire". Although only the top metal layer (Metal 3 for the ON 0.5µm process) is actually used for the connection with the bonding wire, typically the bonding pad is made of all available metal layers stacked on top of each other and interconnected through vias. This arrangement allows connection from the core of the chip to the pad and, in turn, the outside world using any metal layer to interface between the pad and the internal circuit.



The last major processing step in the manufacturing of a wafer is the "passivation" layer (an insulator) that covers the entire chip to protect circuits from environmental contamination or minor damage on the surface. Since the bonding pads need to be accessible for electrical connection to the chip package, this top passivation layer must be removed from the bonding pads. This top passivation layer is termed the *glass* layer. As with all layers in a semiconductor process, the *glass* layer is governed by its own set of design rules.

Note: In the layout the glass layers we create are anywhere this top passivation layer will be cut out to allow electrical contact. So, we place glass layers on the regions where do not want the passivation layer to exist.

Part 2.1: Create the layout of a bonding pad

Create a bonding pad comprised of stacked layers of metal 1-3 with a pad opening in the glass layer. Use stacked vias (stacking of vias is allowed in the AMI06 process) to interconnect these metal layers. To minimize the resistance in the interconnections of these metal layers, use near the maximum possible number of vias, by creating multiple rows and columns, when connecting adjacent metal layers. The pad should be as small as

possible while still meeting design rules but the opening in the glass layer is to be 60µm x 60µm. The opening must lie completely within the pad. This opening requirement is important in determining a lower bound for the area of the pad.

Hint: You can cover the entire surface of a pad with vias efficiently. Use the menu item **Create à Vias** first **Choose Stacked Vias** so you can apply Metal 1-3 vias at the same time and specify the number of **Rows and Columns** of vias you want. You will need to calculate how many rows and columns of vias that you need first.

Part 3: Layout of a diode

In the n-well bulk CMOS process, diodes can be created in two ways: one is with a p+ diffusion in an n-well and the other is with a n+ diffusion in the p-substrate. These two ways of creating a diode are depicted in Figure 2. Though this represents two ways to create a diode, the n+/p-substrate diode has very limited applications since its anode is inherently connected to the substrate. Even the p+/n-well diode has some limitations since there is actually a p-sub/n-well diode also present (but not shown in the figure). The node labels in this figure denote the contacts to the anodes and cathodes of the diodes. For example, the cathode for the p+/n-well diode on the right is actually the n-well or more precisely the n-well region immediately adjacent to the p+ diffusion.

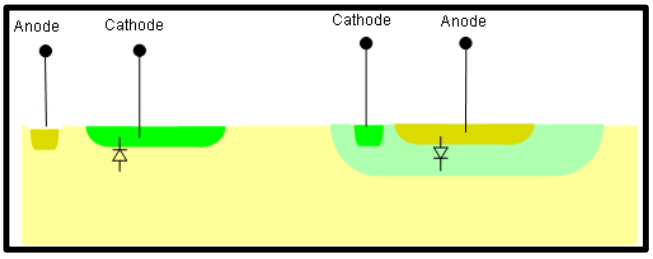


Figure 2:Two Ways to Make Diode in n-well CMOS Process; n+/p-substrate on left and p+/n-well on right

For the purpose of this lab, we will use the p+/n-well diodes and layout each diode in its own n-well, as in Figure 3.

The area factor, A, in the diode equation (1) is the area of the intersection of the diffused regions that form the anode and the cathode. In this layout, the cathode completely surrounds the anode so the area factor, A, is the area of the anode which is formed with the p+ active.

$$I_D = I_S\left(e^{\frac{V_D}{V_t}} - 1\right) = J_S A(e^{\frac{V_D}{V_t}} - 1) \qquad (1)$$

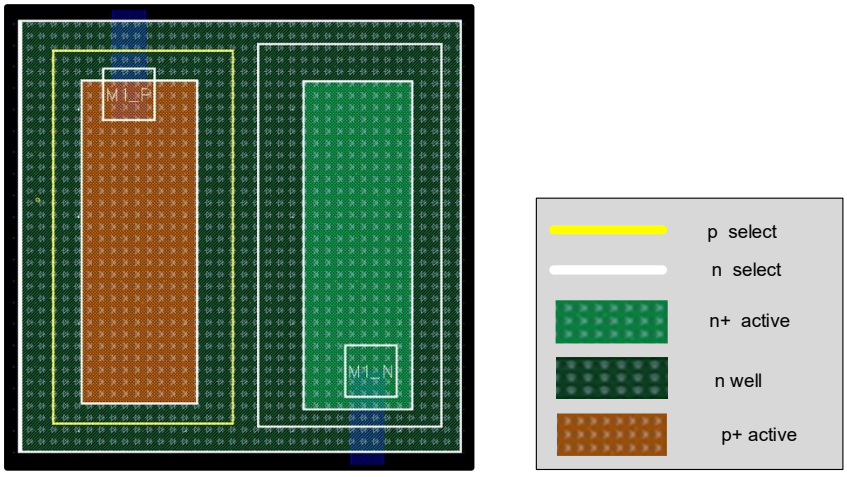


Figure 3: Simple P+ Diode Layout, Cross-sectional View

Similar to the resistor, for extraction of the diode to work correctly, you must completely cover the diffusions used to form the diodes with the cover layer *dio_id* so that the extraction tool recognizes this as a circuit component (i.e. as a diode).

Part 3.1 Create a diode layout

Create the layout for a diode. This diode will be used as part of a pad protection circuit that is discussed in the next section. When used in pad protection circuits, the area of the anode should be quite large. Make a square layout of your diode with the total area about 1/4th that of the bonding pad using the floorplan for the layout shown in Figure 3.

Part 4: Pad Protection Circuitry

Electrostatic discharge (ESD) is a rapid flow of current typically associated with breakdown of air or other gasses. This breakdown is associated with the rapid formation of a plasma. Lightning is one example of electrostatic discharge. If you've ever dragged your feet on carpet so you can shock someone with the tip of your finger, you've created an electrostatic discharge. If the discharge path includes a path through an integrated circuit, the sudden surge of electrons associated with ESD can damage or destroy a circuit. Simply toughing an integrated circuit can cause an ESD event if a person is sufficiently charged such as can occur walking across a carpet or even a dry floor in a low humidity environment. Damage in the integrated circuit occurs because the ESD currents create very large short-term voltages that cause devices in the integrated circuit to fail. In manufacturing environments, there are ways to mitigate the ESD risk by using protocols that may include an ESD smock/wristband/mat, a humidity-controlled environment, and/or ESD safe tools. However, this mitigation does not exist in the real world, where our circuits will most likely operate. Therefore, we need to build in ESD protection into an integrated circuit to protect it from unplanned ESD stress.

Normally, protection circuitry is designed by engineers specializing in ESD protection and is provided to the circuit designers. For the purpose of this lab, you are going to create the simple ESD protection circuit shown in Figure 4. No protection circuits exist to provide protection from all ESD events but some are very effective at providing ESD protection for events that are likely to occur during normal use of an integrated circuit. The simple circuit discussed in this experiment will provide a reasonable level of ESD protection though an actual production circuit may have a much better ESD protection structure. But this circuit is good enough to introduce the

concept of protecting a circuit from ESD damage and good enough to provide some protection from ESD events if included on a fabricated circuit. In this ESD protection circuit the resistor R_{PROT} is to be made of poly and has a ***value of 50 ohms***.

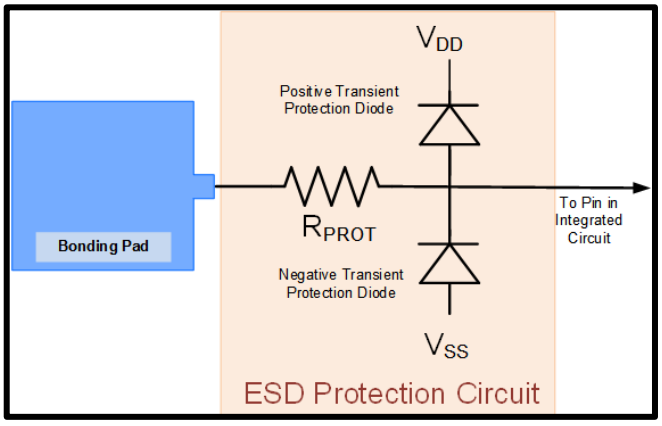


Figure 4: ESD Protection Circuit Schematic

If an ESD event occurs on a bonding pad without ESD protection, the corresponding voltage on the bonding pad can be very large and will propagate directly into the integrated circuit thereby damaging or destroying the IC. But with the ESD protection circuit shown, the actual voltage that gets into the circuit will be limited to about 0.7V above V_{DD} or to about 0.7V below V_{SS}. The excess voltage incident on the bonding pad will be impressed across the resistor R_{PROT}. Many types of resistors can support a large voltage for a short period of time without damaging the resistor. And many diodes can support a large current flow for a short period of time without damaging the diode.

Every pin on the integrated circuit will have a pad protection circuit. Depending upon whether the pin is an input, an output, or a supply voltage, the protection circuit will vary. These variations could be in the size of the resistor, in the size of the diodes, or in some other modifications to the protection circuitry. Pad protection circuits are generally included in a library and the designer simply selects the protection circuit that corresponds to the functionality of each node.

Part 4.1 Create a Pad Protection Schematic

Create a new schematic (call it bondingPadWithESD or something similar) and recreate the schematic of the ESD protection circuit (the Bonding Pad is just an input pin in this schematic). This schematic will be used for LVS later.

Part 5: Layout of the bonding pad with protection circuit

Create a layout of a bonding pad with an ESD protection circuit. Instantiate the needed components in the bonding pad design (we made most of these in other parts of the lab). Make sure your layout passes DRC and LVS. Build a symbol for this protection circuitry.

Attempting to run a simulation of this ESD protection will not work. This is because the computer does not have a model for the diodes. You will need to create a diode model that tells the software how to model the diode in the schematic. To do so, go to the folder containing your diode (cd ~/ee330/{lab library}/diode, or something similar) and create a text file called **diode.scs** (gedit diode.scs) and include the following text:

```
simulator lang = spectre

library dio
section d
model diode diode is=1.8e-12 rs=1.43 n=1.22
endsection d
endlibrary dio
```

You will need to add this model to a simulation later.

Part 5.1: Human Body Model

The human body model is an electrical equivalent of a human touching a circuit to induce static discharge. It is modeled as a 100pF capacitor discharging through a 1500 ohm resistor in series to the device under test (DUT). The human body model (HBM) is shown in Figure 5. Devices are qualified into different classes depending upon how much voltage they can handle from this configuration. This of course corresponds to how much static electricity you build up before touching your device! The different classes can be found in Figure 7.

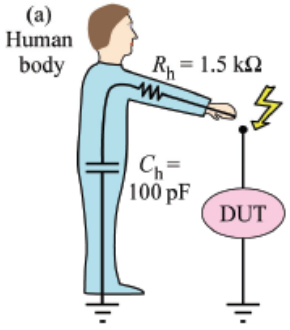


Figure 5: HBM

Create a new schematic and call it **HBM_TB**. Add the human body model and your protection circuitry. Remember to hook up Vss and Vdd. Simulate the circuit assuming the output of the protection circuit is loaded with a 1pF capacitor. Set the starting voltage of the charged capacitor using the 'Initial Conditions' query in the properties of the 100pF capacitor. Set the starting voltage of the 1pF load capacitor to 0V.

Before simulating your test circuit, you must include the diode file created earlier in the model. To do this, open ADE Assembler, create a test for your schematic, and go to Setup Model Libraries and a popup will appear like figure 6. Click on the (…) button to the right of <Click here to add model file> then find your diode.scs file in your file system. Click on the section area to the right of this and a small down arrow will appear. Click on the drop down list and select, “d”.

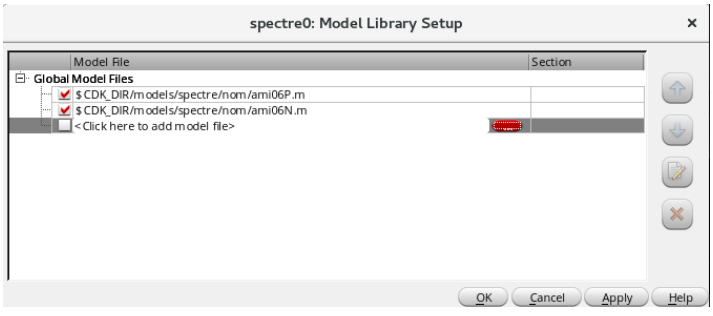


Figure 6: Including Model Libraries

Run the circuit for a variety of starting voltages and see how the protection circuitry works. If we specify Vdd = 3.3V and any voltage above 5V destroys the circuitry (a capacitor in this simulation), to what class of devices would this belong? How could you improve the protection of the circuit?

Class	ESD withstand voltage, V_w
0	0 ~ 250 V
1A	250 ~ 500 V
1B	500 ~ 1000 V
1C	1000 ~ 2000 V
2	2000 ~ 4000 V
3A	4000 ~ 8000 V
3B	> 8000 V

Figure 7: HBM Classifications

Appendix 1

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS	K		UNITS
Inverters			
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate

COMMENTS: SUBMICRON

T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

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+DWB     = 3.676235E-8    VOFF     = -1.493503E-4    NFACTOR  = 1.0354201
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+DSUB    = 0.0764123      PCLM     = 2.5941582       PDIBLC1  = 0.8187825
+PDIBLC2 = 2.366707E-3    PDIBLCB  = -0.0431505      DROUT    = 0.9919348
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+UB1     = -7.61E-18      UC1      = -5.6E-11        AT       = 3.3E4
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+WWN     = 1              WWL      = 0               LL       = 0
+LLN     = 1              LW       = 0               LWN      = 1
+LWL     = 0              CAPMOD   = 2               XPART    = 0.5
+CGDO    = 2.32E-10       CGSO     = 2.32E-10        CGBO     = 1E-9
+CJ      = 4.282017E-4    PB       = 0.9317787       MJ       = 0.4495867
+CJSW    = 3.034055E-10   PBSW     = 0.8             MJSW     = 0.1713852
+CJSWG   = 1.64E-10       PBSWG    = 0.8             MJSWG    = 0.1713852
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+CDSCB    = 0               ETA0     = 0.4060383       ETAB    = -0.0633609
+DSUB     = 1               PCLM     = 2.2703293       PDIBLC1 = 0.0279014
+PDIBLC2  = 3.201161E-3     PDIBLCB  = -0.057478       DROUT   = 0.1718548
+PSCBE1   = 4.876974E9      PSCBE2   = 5E-10           PVAG    = 0
+DELTA    = 0.01            RSH      = 105.3           MOBMOD  = 1
+PRT      = 0               UTE      = -1.5            KT1     = -0.11
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+UB1      = -7.61E-18       UC1      = -5.6E-11        AT      = 3.3E4
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+WWN      = 1               WWL      = 0               LL      = 0
+LLN      = 1               LW       = 0               LWN     = 1
+LWL      = 0               CAPMOD   = 2               XPART   = 0.5
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